Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Canceled)

2. (Previously Presented) A phase comparator circuit for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that;

said data signal is inputted to a first latch circuit and a second latch circuit, said first latch circuit performs the latching operation thereof with a first clock signal, and said second latching circuit performs the latching operation thereof with the second clock signal, as being an inverted clock signal of said first clock signal;

the output of said first latching circuit is inputted to a third latch circuit, the output of said second latch circuit is inputted to a fourth latch circuit, said third latch circuit performs the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal;

the output of said second latch circuit is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as a first phase error signal; and

the output of said first latch circuit is connected to a second delay circuit, an exclusive OR of the output from said second delay circuit and the output from said fourth latch circuit is used as a second phase error signal.

3 - 9. (Canceled)

10. (Currently Amended) A CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, and said phase comparator circuit characterized in that;

said data signal is inputted to a first latch circuit and a second latch circuit, said first latch circuit performs the latching operation thereof with a first clock signal, and said second latching circuit performs the latching operation thereof with the second clock signal, as being an inverted clock signal of said first clock signal;

the output of said first latching circuit is inputted to a third latch circuit, the output of said second latch circuit is inputted to a fourth latch circuit, said third latch circuit performs the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal;

the output of said second latch circuit is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as first phase error signal;

the output of said first latch circuit is connected to a second delay circuit, an exclusive OR of the output from said second delay circuit and the output from said fourth latch circuit is used as a second phase error signal; and

said first and second phase error signals are outputted to said charge pump circuit.

11 - 12. (Canceled)